AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Fernando Gonzalez et al.	§	Group Art Unit: 2814
Serial No.: 10/081,915	§	Examiner: Peralta, Ginette
Filed: February 22, 2002	§	
For: METHOD FOR FORMING CONDUCTORS IN A SEMICONDUCTOR DEVICE	§	Atty. Docket: MCRO:125--4/FLE 94-0281.04

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June 6, 2005 — Date
Michael G. Fletcher

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in furtherance to the Notice of Appeal mailed on April 1, 2005, and received by the Patent Office on April 6, 2005.

1. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., the Assignee of the above-referenced application by virtue of the Assignment recorded at reel 7889, frame 0678, and dated February 23, 1996.

2. **RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellants' legal representative in this Appeal. Micron Technology, Inc., the Assignee of the above-referenced application, as evidenced by the documents mentioned above, will be directly affected by the Board's decision in the pending appeal.

3. **STATUS OF CLAIMS**

Claims 18-60 are currently pending, and claims 19, 20, 35-36, 40-49, and 53-60 are currently under final rejection and, thus, are the subject of this Appeal. The remaining claims have been withdrawn from consideration as being directed to a non-elected species. Therefore, Appellants respectfully request allowance of such claims upon allowance of a generic claim.

4. **STATUS OF AMENDMENTS**

The Response to Official Action, mailed on August 5, 2004, has been entered, and no response to the Final Official Action of November 1, 2004, was filed. Therefore, the present application is not subject to any pending amendments.

5. **SUMMARY OF CLAIMED SUBJET MATTER**

The present application currently contains two independent claims that are subject to this appeal, claims 19 and 20. To explain the subject matter defined by independent claims 19 and 20, specific embodiments within the scope of these claims are identified in the specification. However, it is important to note that the embodiments subsequently discussed merely explain subject matter falling within the scope of the claims at issue, rather than defining the scope of the

claims itself. Thus, while the following embodiments are exemplary of claims 19 and 20, they are not definitive.

Independent claim 19, the first of two independent claims subject to the present appeal, recites:

> A method for making a memory device, comprising the steps of:
>
> providing a substrate having a first conductive line therein;
> forming a plurality of memory cells, each said memory cell comprising an element programmable to multiple states of resistance;
> forming a second conductive line, said second conductive line in electrical communication with one of said memory cells; and
> creating a third conductive line in electrical communication with said first conductive line and said plurality of memory cells.

The method of claim 19, in one embodiment, results in a memory cell with variable resistance that is electrically accessible through dual complimentary digit lines, the first conductive line and the third conductive line, wherein the first conductive line is buried in the substrate. The following identifies the contribution of each step listed in claim 19 toward the construction of this embodiment. The step of "providing a substrate having a first conductive line therein" provides the first digit line 7. *See* Application, p. 9, ll. 11-12. As depicted in FIG. 1A and 1B, the first digit 7 line is formed in the substrate by selectively doping a linear strip of a semiconductor. *See* Application, p. 9, ll. 6-12. On top of this substrate with its linear conductive region, there are formed multiple programmable resistors made of chalcogenide 50, which changes resistance in response to a large programming current but remains unaltered by a small read current. *See* Application, p. 11, ll. 22 - p. 12, ll. 2; FIG. 8. In this embodiment, each memory cell includes only one programmable resistor, which connects to the first digit line through a diode. The second conductive line, a word line 60 in this embodiment, is formed over

the memory cells such that it runs in a direction perpendicular to the first digit line. *See* Application, p. 12, ll. 4-7; FIG. 8. In the last step listed in the claim, the third conductive line, a complimentary digit line 85 in this embodiment, is formed above the word line 60 and parallel to the first digit line 7 formed in the substrate. *See* Application, p. 12, ll. 21-25; FIG. 8. The upper digit line 85 connects to the doped regions of the substrate forming the first digit line 7 through plugs 40. The dual digit lines 7 and 85 serve to reduce the resistance when accessing the programmable memory cells, as the programming current can be relatively large and small changes in resistance may be difficult to read when the interconnect resistance is high.

Turning to the second independent claim subject to the present appeal, independent claim 20 recites:

> A method for forming a memory array, comprising the steps of:
>
> forming a digit line in a substrate;
>
> forming a plurality of memory cells in a first insulative layer, said memory cells overlying said digit line and in electrical communication with said digit line, each memory cell comprising an element having an alterable resistance, said first insulative layer having an opening therein;
>
> forming a contact plug in said opening, said plug in electrical communication with said digit line;
>
> forming a plurality of first conductive lines disposed with one of said first conductive lines overlying and in electrical communication with a selected one of said memory cells; and
>
> forming a second conductive line in a second conductive layer, said second conductive line in electrical communication with said contact plug.

As with the previous claim, independent claim 20 is explained by identifying the contribution of each step listed in claim 20 toward the construction of an exemplary embodiment

described in the specification. One embodiment of claim 20 produces variable resistance memory cells accessible through dual digit lines located above and below the memory cells. The step of "forming a digit line in a substrate" produces a substrate with a linear doped region that acts as a conductive line 100. *See* Application, p. 14, ll. 1-3; FIGS. 9A-B. Over, along, and in electrical contact with this linear doped region, the second claimed step forms multiple memory cells that store information in a programmable resistor 193. *See* Application, p. 18, ll. 5-14; FIG. 17B. The third step listed, in this embodiment, forms contact plugs 170 that connect the lower digit line 100 to the complimentary upper digit line formed in the last step listed in the claim. *See* Application, p. 16, ll. 18-20; FIG. 16. The fourth step listed forms word lines 215, running perpendicular to the digit lines, and placing each programmable resistor in series with a unique word line and digit line combination. *See* Application, p. 18, ll. 23-24; FIG. 19B. The last step listed in claim 20, in this embodiment, provides a supplemental digit line 230, or strapping layer, to reduce the read and programming resistance. *See* Application, p. 19, ll. 10-13; FIG. 21B.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Independent Claim 19 and the Claims Depending Therefrom

Appellants respectfully urge the Board to review and reverse the Examiner's rejection of claims 19, 35, 36, and 40-47 under 35 U.S.C. § 103(a) as being unpatentable over the Ikeda et al. reference (U.S. Pat. 5,731,219, hereinafter "Ikeda") in view of the Brickman et al. reference (U.S. Pat. 3,721,838, hereinafter "Brickman").

Independent Claim 20 and the Claims Depending Therefrom

Appellants respectfully urge the Board to review and reverse the Examiner's rejection of claims 20, 48, 49, and 53-60 under 35 U.S.C. § 103(a) as being unpatentable over Ikeda in view

of Brickman and further in view of the Gonzalez et al. reference (U.S. Pat. 5,150,276, hereinafter "Gonzalez").

7. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. The Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under Section 103(a). Appellants strongly believe that this application should have been allowed in view of the response filed on August 5, 2004. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 19, 20, 35, 36, 40-49, and 53-60 are currently in condition for allowance.

More specifically, with respect to both Section 103 rejections, Appellants note that the burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). To establish a *prima facie* case, the Examiner must show both that the combination includes *all* of the claimed elements and a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

Independent Claim 19 and the Claims Depending Therefrom

In the Office Action, mailed November 1, 2004, with respect to claim 19, the Examiner stated:

> Claim[s] 19, 35, 36, and 40-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Pat. 5,731,219) in view of Brickman et al. (U.S. Pat. 3,721,838) as applied before.
>
> Ikeda et al. discloses [sic] in [FIGS]. 9, and 26-32, a method for making a memory device that comprises providing a substrate having a first conductive line 13 therein; forming a plurality of memory cells; forming a second conductive line 29, the second conductive line 29 in electrical communication with one of the memory cells; and creating a third conductive line 33 in electrical communication with the first conductive line and the plurality of memory cells, wherein the third conductive line 33 is created for the well known and disclosed intended purpose of connecting the memory cells to other areas of the circuit.
>
> Ikeda et al. discloses [sic] the claimed invention with the exception of forming the memory cells comprising an element programmable to multiple states of resistance.
>
> Brickman et al. discloses [sic] in [FIGS]. 1 and 5 a method for making a memory device that comprises providing a substrate having a first conductive line 52 therein; forming a plurality of memory cells, each memory cell comprising an element **S** [emphasis in origional] programmable to multiple states of resistance, wherein the memory cells comprising an element **S** programmable to multiple states of resistance is formed for the disclosed intended purpose of being used in different states by electrically altering the element when another element of the memory cell array is disabled or deactivated.
>
> Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell comprising an element programmable to multiple states of resistance, wherein the element is formed as part of the memory cell for the disclosed intended purpose of being used in different states by electrically altering the element when another element of the memory cell array is disabled or deactivated as shown by Brickman et al. and as it may be applied to the invention of Ikeda et al.

Iindependent claim 19 recites, *inter alia*, "a substrate having a first conductive line *therein*," a "*memory cell* comprising an element programmable to multiple states of resistance," and "a third conductive line in electrical communication with said first conductive line." (Emphasis added.) Despite the Examiner's assertion that Ikeda discloses all elements of claim 19 except a memory cell comprising an element with programmable resistance, Ikeda does not teach *a conductive line in the substrate*. Although the cited reference teaches a conductive region (the active area) in the substrate, and although the reference teaches conductive lines, the reference does not teach a conductive line *in* the substrate. The active areas of the substrate taught by the Ikeda reference are clearly not lines. Instead, Fig. 15 of Ikeda illustrates the *ring* shape of the doped region in the substrate 1. Ikeda, col. 36, ll. 53-55. Accordingly, the conductive region in the substrate disclosed by Ikeda is not a conductive line. As further proof that Ikeda does *not* teach conductive lines in the substrate, the Ikeda reference teaches field oxide 4 completely surrounding each active area. Ikeda, Fig. 15. The field oxide 4 would block any conductive line in the substrate between memory cells. Indeed, nothing in the Ikeda reference suggests creating a conductive line in the substrate. Of the three conductive lines cited by the Examiner in the Office Action, the word line (WL) 13, the sub-word line (SWL) 29, and the data line (DL) 33, none are located *in the substrate* as recited in claim 19. Accordingly, the Ikeda reference fails to disclose a substrate having a first conductive line *therein*, as called for in claim 19.

In response to this argument, in the Office Action, the Examiner merely alleged that "the conductive line 13 of Ikeda is within the substrate limits and bounds."

Appellants disagree with the Examiner's assertion that this reference teaches a substrate with a conductive line *therein*. As stated above, the conductive line identified by the Examiner rests *on* the substrate, not in the substrate. Moreover, merely asserting that the conductive line is "within the limits and bounds" does not constitute *objective evidence* that the reference teaches a conductive line *in* the substrate. Accordingly, without unreasonably extending the meaning of a substrate having a first conductive line *therein* to encompass a substrate with conductive lines *thereon*, this reference fails to teach all the features of claim 19.

Moreover, the Examiner's assertion that Brickman discloses " a substrate having a first conductive line 52 therein" is similarly baseless. As FIG. 5 of Brickman clearly illustrates, the line 52 identified by the Examiner is clearly above the substrate 38. Indeed, the conductive line 52 taught by Brickman is separated from the substrate by oxidation layer 39. Thus, Brickman fails to teach a conductive line that even contacts the substrate, let alone a conductive line *in* the substrate.

Secondly, the Brickman reference fails to disclose the element of claim 19 for which it was cited by the Examiner: "a *memory cell* comprising an element programmable to multiple states of resistance." The Brickman reference teaches a fuse capable of providing two states of resistance that is not *part of* a memory cell. *See* Brickman, col. 2, ll. 15-22. The fuse taught by Brickman disables damaged portions of memory and allows access to redundant memory arrays. While the fuse in Brickman is electrically alterable, the circuit in which it is comprised serves none of the other functions of memory; for example, the circuit does not return stored information to other areas of the device. In fact, the operation of the circuit is invisible to other areas of the device. *See* Brickman, col. 2, ll. 22-23. Moreover, the Brickman reference

explicitly distinguishes between the circuit comprising the fuse and a memory cell, explaining that "[s]ince the present invention is directed to an alterable decoder, further description of the memory operation is not believed necessary." Brickman, col. 5, ll. 33-35. Thus, the cited reference fails to disclose any memory cell, much less a memory cell comprising an element programmable to multiple states of resistance.

In response to this argument, in the Office Action mailed November 1, 2004, the Examiner stated:

> Regarding the [A]pplicant's argument that the Brickman reference fails to disclose the claimed element of 'a memory cell programmable to multiple states of resistance' it is noted that the claim language refers to "each said memory cell comprising an element programmable to multiple states of resistance" and that Brickman teaches within a memory cell an element programmable to multiple states of resistance and it is for this element that the reference is relied upon.

However, beyond the Examiners bare assertion, there is no evidence to suggest that the fuse taught by Brickman is *a memory cell*. Instead, Brickman teaches a fuse that is part of a circuit for disabling damaged portions of memory. The Examiner still has provided no evidence that this portion of the circuitry is actually a memory cell, and Appellants note the Examiner's continued failure to point to any portion of the reference that suggests the circuit comprising the fuse stores and returns data.

Finally, either the Ikeda reference does not teach "a third conductive line in electrical communication with said first conductive line," as called for in claim 19, or the Ikeda reference

as explained by the Examiner is inoperative. In the Office Action, the Examiner asserted that Ikeda teaches "a third conductive line 33 in electrical communication with the first conductive line [13]." However, if the Examiner is correct, the device taught by Ikeda short circuits around the memory cell, thus rendering the memory cell inoperative. Office Action, pg. 2. Ikeda teaches a SRAM with a memory cell in series between the first conductive line 13 and the third conductive line 33. Thus, if the first conductive line 13 connects directly to the third conductive line 33, the memory cell cannot receive or return data. Specifically, the Ikeda reference identifies the first conductive line 13 as a word line (WL) 13 in column 37 lines 13-15 and the third conductive line 33 as a data line (DL) 33 in column 51 lines 22-32. Fig. 5 of Ikeda provides an electrical schematic illustrating the position of the memory cell in series between the data lines 33 and the word lines 13. If a word line 13 is in direct electrical communication with a data line 33, the memory device is short circuited, rendering it incapable of returning or storing information. Thus, either the Examiner did not identify a third conductive line in electrical communication with a first conductive line, or the Ikeda reference is inoperative.

In response to this argument, in the Office Action mailed November 1, 2004, the Examiner wrote:

> Regarding the [A]pplicant's argument that either the Ikeda reference does not teach a "third conductive line in electrical communication with said first conductive line and said plurality of memory cells" or the Ikeda reference as explained by the [E]xaminer is inoperative, as it shorts circuits around the memory cell, it is noted that the third conductive line 33 is in electrical communication with the conductive line 13... [I]t is not the [E]xaminer's positon[,] or what Ikeda proposes[,] that the third conductive line 33 is in *direct electrical communication* [emphasis in origional] with the conductive line 13, as seen in [FIG]. 9 ... [W]hat is taught by Ikeda is that the conductive line 33 is in

> electrical communication with the conductive line 13 through the source electrode of the conductive line 13, there is no direct electrical communication, and the claim language does not exclude an indirect electrical communication.

Appellants strongly disagree with the Examiners interpretation of the phrase "in electrical communication" with respect to the operation of the SRAM memory cell taught by Ikeda: "the conductive line 33 is in electrical communication with the conductive line 13 through the source electrode of the conductive line 13." Office Action mailed November 1, 2004, page 9. As explained above, the conductive line 13 is a word line and the conductive line 33 is a digit line. Ikeda, col. 37, ll. 13-15; and col. 51, ll. 22-32. Appellants note the Examiner's failure to contest this point and can only assume the Examiner agrees. As clearly indicated in FIG. 5 of Ikeda, the word lines 13 (WL1 and WL2) are separated from the digit lines 33(DL1 and DL2) by the gate oxide of field effect transistors Qt1 and Qt2. *See* Ikeda, Abstract (indicating that the memory cell is composed of MISFETs). Thus, the Examiner has asserted that one conductor, the word line 13, is in electrical communication with another conductor, the digit line 33, through an insulator, the gate oxide of field effect transistors Qt1 and Qt2. While the Examiner is entitled to give the phrase "in electrical communication" its broadest reasonable interpretation, interpreting it to encompass two conductors between which no current flows, as is the case with the source and gate of a field effect transistor, is clearly unreasonable.

Therefore, Appellants respectfully assert that independent claim 19 and its respective dependent claims 35, 36, and 40-47 are not rendered obvious by the cited references. With the foregoing in mind, Appellants respectfully request reconsideration and allowance of the instant claims.

Independent Claim 20 and the Claims Depending Therefrom

In the Office Action mailed November 1, 2004, the Examiner stated:

> Claims 20, 48, 49, and 53-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. in view of Brickman et al. and Gonzales et al. (U.S. Pat. 5,150,276).
>
> Ikeda et al. discloses [sic] in [FIGS]. 9, and 26-32, a method for making a memory device that comprises providing a substrate having a first conductive line 13 therein; forming a plurality of memory cells; forming a second conductive line 29, the second conductive line 29 in electrical communication with one of the memory cells; and creating a third conductive line 33 in electrical communication with the first conductive line and the plurality of memory cells, wherein the third conductive line 33 is created for the well known and disclosed intended purpose of connecting the memory cells to other areas of the circuit.
>
> Ikeda et al. discloses [sic] the claimed invention with the exception of forming the memory cells comprising an element programmable to multiple states of resistance, the first conductive line being a digit line, forming a contact plug in an opening in the dielectric layer, and forming a conductive line in a second conductive layer, the conductive line being in electrical communication with the contact plug.
>
> Brickman et al. discloses [sic] in [FIGS]. 1 and 5 a method for making a memory device that comprises providing a substrate having a first conductive line 52 therein; forming a plurality of memory cells, each memory cell comprising and element **S** [emphasis in origional] programmable to multiple states of resistance, wherein the memory cells comprising and element **S** programmable to multiple states of resistance is formed for the disclosed intended purpose of being used in different states by electrically altering the element when another element of the memory cell array is disabled of deactivated.
>
> Thus[,] it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell comprising an element programmable to multiple states of resistance, wherein the element is formed as part of the memory cell for the disclosed intended purpose of being used in different states by electrically altering the element when another element of the memory cell array is disabled or deactivated as shown by Brickman et al. and as it may be applied to the invention of Ikeda et al.

> Gonzales et al. discloses [sic] in F[IG]. 15 and in cols. 5 to 9, a method of making a memory array, that includes forming a contact plug 175 in an insulating layer 40[,] wherein the memory cells are formed, forming a plurality of first conductive lines 130 disposed with one of the first conductive lines overlying and in electrical communication with a selected one of the memory cells; and forming a second conductive ine 190 in a second conductive layer, the second conductive line 190 in electrical communication with the contact plug 175, wherein Gonzales et al. further teaches that it is well known in the art the placing of word lines and digit lines beneath the capacitive layer (col. 2, ll. 3-21), and wherein a plurality of contact plugs are formed in the insulating layer between respective pair of memory cells, and conductive lines are formed in electrical communication with the contact plugs for the disclosed intended purpose of providing electrical communication between the contact plugs and the peripheral contacts of the cell array.
>
> Thus[,] it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a digit line in the substrate in a multilevel structure in order to interconnect various levels of the array and to form a contact plug and a conductive line in electrical communication with the contact plug in order to provide electrical communication between the contact plug, and therefore the memory cells, and the peripheral contacts of the cell array.

In contrast, independent claim 20 recites, *inter alia*, "forming a digit line *in* a substrate," and "each *memory cell* comprising an element having an alterable resistance." (Emphasis added.)

As discussed above, the cited references fail to disclose a digit line *in* the substrate. For example, all conducting lines taught by Ikeda are above the substrate, not in it. Moreover, the doped, and therefore potentially conducting, region of the substrate taught by Ikeda is in the shape of a ring, not a line. Nothing in Ikeda even suggests creating doped lines in the substrate. Indeed, the three conductive lines, the word line 13, the sub-word line 29, and the data line 33,

cited by the Examiner as corresponding to the conductive lines of the instant claim are all clearly above, not in, the substrate. Ikeda, Fig. 9. Further, the conductive line 52 in Brickman that the Examiner identified as in the substrate clearly is above or on the substrate. Moreover, Appellants note that the Examiner does not even suggest that Gonzales teaches this feature. Thus, the cited references do not teach forming a digit line *in* the substrate.

Secondly, and again as discussed above, the Brickman reference does not disclose a "*memory cell* comprising an element having an alterable resistance," as called for in claim 20. (Emphasis added.) Brickman discloses a circuit comprising a *fuse* with alterable resistance used to disable damaged portions of memory, not a memory cell used to store and return data. Indeed, the cited reference teaches that the fuse should not return information to other areas of the circuit. Moreover, the cited reference itself distinguishes between this circuit comprising the fuse and a memory cell, further illustrating that they are not interchangeable parts. Furthermore, Appellants note that the Examiner does not even suggest that Gonzales or Ikeda teach this feature. Accordingly, the Brickman reference fails to disclose a *memory cell* with an element having alterable resistance.

Therefore, Appellants respectfully assert that independent claim 20 and its respective dependent claims, 48, 49, and 53-60, are not rendered obvious by the cited reference. With the foregoing in mind, Appellants respectfully request reconsideration and allowance of the instant claims.

9. **CONCLUSION**

In view of the above remarks, Appellants respectfully submit that the Examiner has provided no supportable position or evidence that claims 19, 20, 35, 36, 40-49, and 53-60 are obvious under Section 103(a). Accordingly, Appellants respectfully request that the Board find claims 19, 20, 35, 36, 40-49, and 53-60 patentable over the prior art of record, withdraw all outstanding rejections, and allow claims 19, 20, 35, 36, 40-49, and 53-60.

In accordance with 37 C.F.R. § 1.136, Appellants request that this and any future reply requiring an extension of time be treated according to the General Authorization For Extensions Of Time previously submitted.

The Commissioner is authorized to charge the requisite fee of $500.00, and any additional fees which may be required, to Deposit Account No. 13-3092; Order No. MCRO:125-4/FLE (94-0281.04).

Respectfully submitted,

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10. **APPENDIX OF CLAIMS ON APPEAL**

19. (original) A method for making a memory device, comprising the steps of:

providing a substrate having a first conductive line therein;

forming a plurality of memory cells, each said memory cell comprising an element programmable to multiple states of resistance;

forming a second conductive line, said second conductive line in electrical communication with one of said memory cells; and

creating a third conductive line in electrical communication with said first conductive line and said plurality of memory cells.

20. (original) A method for forming a memory array, comprising the steps of:

forming a digit line in a substrate;

forming a plurality of memory cells in a first insulative layer, said memory cells overlying said digit line and in electrical communication with said digit line, each memory cell comprising an element having an alterable resistance, said first insulative layer having an opening therein;

forming a contact plug in said opening, said plug in electrical communication with said digit line;

forming a plurality of first conductive lines disposed with one of said first conductive lines overlying and in electrical communication with a selected one of said memory cells; and

forming a second conductive line in a second conductive layer, said second conductive line in electrical communication with said contact plug.

35 (previously presented). The method, as set forth in claim 19, comprising the step of:

forming a plurality of contacts between the first conductive line and the third conductive line, a respective one of the plurality of contacts being formed between respective pairs of memory cells.

36 (previously presented). The method, as set forth in claim 19, wherein the step of providing the first conductive line comprises the step of:

forming a titanium silicide layer over the first conductive line.

37 (withdrawn). The method, as set forth in claim 19, wherein the step of forming a plurality of memory cells comprises the steps of:

for each of the memory cells, forming an access device having a first terminal and a second terminal, the first terminal being in electrical communication with the first conductive line; and

for each of the memory cells, forming the element in electrical communication with the second terminal of the access device.

39 (previously presented). The method, as set forth in claim 37, wherein the step of forming the element comprises the step of:

forming a chalcogenide memory element.

40 (previously presented). The method, as set forth in claim 19, wherein the step of forming a plurality of memory cells comprises the step of:

forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit.

41 (previously presented). The method, as set forth in claim 40, wherein the step of forming a plurality of memory cells comprises the step of:

forming pairs of memory cells, each pair being spaced apart by a distance approximately equal to the minimum photolithographic limit.

42 (previously presented). The method, as set forth in claim 35, wherein the step of forming a plurality of contacts comprises the step of:

forming each contact from a doped semiconductive region of the substrate.

43 (previously presented). The method, as set forth in claim 35, wherein the step of forming a plurality of contacts comprises the steps of:

forming dielectric spacers between each pair of memory cells; and

forming each contact between the respective dielectric spacers.

44 (previously presented). The method, as set forth in claim 43, wherein each contact and its respective dielectric spacers have a combined width approximately equal to a minimum photolithographic limit.

45 (previously presented). The method, as set forth in claim 35, wherein the step of forming a third conductive line comprises the step of:

isolating each of the plurality of memory cells from the plurality of contacts.

46 (previously presented). The method, as set forth in claim 45, wherein the step of isolating comprises the step of:

disposing dielectric material on each of the plurality of memory cells.

47 (previously presented). The method, as set forth in claim 46, wherein the step of forming the third conductive line comprises the step of:

forming the third conductive line through tapered holes extending through the dielectric material to the contacts.

48 (previously presented). The method, as set forth in claim 20, comprising the step of:

forming a plurality of contact plugs between the digit line and the second conductive line, a respective one of the plurality of contact plugs being formed between respective pairs of memory cells.

49 (previously presented). The method, as set forth in claim 20, wherein the step of forming the digit line comprises the step of:

forming a titanium silicide layer over the digit line.

52 (previously presented). The method, as set forth in claim 50, wherein the step of forming the element comprises the step of:

forming a chalcogenide memory element.

53 (previously presented). The method, as set forth in claim 20, wherein the step of forming a plurality of memory cells comprises the step of:

forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit.

54 (previously presented). The method, as set forth in claim 20, wherein the step of forming a plurality of memory cells comprises the step of:

forming pairs of memory cells, each pair being spaced apart by a distance approximately equal to the minimum photolithographic limit.

55 (previously presented). The method, as set forth in claim 48, wherein the step of forming a plurality of contact plugs comprises the step of:

forming each contact plug from a doped semiconductive region of the substrate.

56 (previously presented). The method, as set forth in claim 48, wherein the step of forming a plurality of contact plugs comprises the steps of:

forming dielectric spacers between each pair of memory cells; and

forming each contact plug between the respective dielectric spacers.

57 (previously presented). The method, as set forth in claim 56, wherein each contact plug and its respective dielectric spacers have a combined width approximately equal to a minimum photolithographic limit.

58 (previously presented). The method, as set forth in claim 48, wherein the step of forming a second conductive line comprises the step of:

isolating each of the plurality of memory cells from the plurality of contact plugs.

59 (previously presented). The method, as set forth in claim 58, wherein the step of isolating comprises the step of:

disposing dielectric material on each of the plurality of memory cells.

60 (previously presented). The method, as set forth in claim 59, wherein the step of forming the second conductive line comprises the step of:

forming the second conductive line through tapered holes extending through the dielectric material to the contact plugs.